AMENDMENTS TO THE CLAIMS

1-17 (canceled)

18. (previously presented) A stacked microelectronic device, comprising:

a first substrate of silicon, said first substrate having a top surface;

a first plurality of interconnect structures formed on at least a portion of the first substrate;

a layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate of silicon, at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures; and

a second substrate of silicon with a second plurality of interconnect structures formed thereon, said first and second substrates configured such that at least a portion of the interconnect structures of said first and second substrates respectively are in physical contact.

19. (previously presented) The device of claim 18, wherein the device comprises a stacked chipset.

20. (previously presented) The device of claim 18, wherein the first and second substrates comprise integrated circuits.

21. (previously presented) The device of claim 18, wherein at least a portion of the first plurality of interconnect structures or the second plurality of interconnect structures comprise copper vias.

22. (previously presented) The device of claim 18, wherein the compliant material substantially comprises a soft polymer.

23. (previously presented) The device of claim 18, wherein the compliant material substantially comprises one of polyimide, polybenzoxazole, photodefinable siloxane, novolak, or a polynorborene buffer.

24. (previously presented) The device of claim 18, wherein the compliant material comprises photodefinable and non-photodefinable materials.

25-37. (canceled)

38. (new) A stacked device, comprising:

a first substrate having a top surface;

a first plurality of interconnect structures formed on at least a portion of the first substrate;

a first layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate, at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures; and

a second substrate with a second plurality of interconnect structures formed thereon, said first and second substrates configured such that at least a portion of the interconnect structures of said first and second substrates respectively are in direct physical contact.

39. (new) The device of claim 38, further comprising:

a second layer of nonconductive compliant material disposed between the first layer of nonconductive compliant material and the second substrate, the second layer of nonconductive compliant material in direct physical contact with the second substrate.

40. (new) The device of claim 39, wherein a portion of the second layer of nonconductive compliant material opposing the top surface of the first layer of nonconductive compliant material is in direct physical contact with the top surface of the first layer of nonconductive compliant material.

41. (new) The device of claim 40, wherein the portion of the second layer of nonconductive compliant material is compressed.

42. (new) The device of claim 38, wherein the top surface of the first layer of nonconductive compliant material is angled such that a second portion of the layer of nonconductive compliant material has a surface in direct physical contact with the second substrate.

43. (new) The device of claim 42, wherein the second portion of the layer of nonconductive compliant material having a surface in direct physical contact with the second substrate comprises the second portion of the layer of nonconductive compliant material having a surface in direct physical contact with a dielectric layer of the second substrate.

44. (new) The device of claim 38, wherein the first layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate comprises the first layer of nonconductive compliant material formed on at least a portion of a top surface of a dielectric layer of the first substrate.

45. (new) A device, comprising:

a first substrate having a top surface, the first substrate comprising a microelectronic die having an active surface;

a first plurality of interconnect structures formed on at least a portion of the active surface of the first substrate;

a layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate, at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures; and

a second substrate with a second plurality of interconnect structures formed thereon, said first and second substrates stacked such that at least a portion of the interconnect structures of said first and second substrates respectively are in direct physical contact, the layer of nonconductive compliant material structurally supporting the stacked substrates.

46. (new) The device of claim 45, wherein the top surface of the layer of nonconductive compliant material is angled such that a second portion of the layer of nonconductive compliant material has a surface in direct physical contact with the second substrate.

47. (new) The device of claim 46, wherein the second portion of the layer of nonconductive compliant material having a surface in direct physical contact with the second substrate comprises the second portion of the layer of nonconductive compliant material having a surface in direct physical contact with a dielectric layer of the second substrate.

48. (new) The device of claim 45, wherein the first substrate comprises a material selected from the group consisting of: germanium, indium telluride, or gallium antimonide.

49. (new) The device of claim 45, wherein the first layer of nonconductive compliant material is a polymer.

50. (new) The device of claim 45, wherein the layer of nonconductive compliant material structurally supporting the stacked substrates includes a portion of the layer being compressed between the stacked substrates.